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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/755,164	01/08/2001	Nestor A. Bojarczuk, JR.	YOR9-2000-0642	4431

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EXAMINER	
QUINTO, KEVIN V	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/755,164	BOJARCZUK, ET AL.	
	Examiner	Art Unit	
	Kevin Quinto	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7,14-18 and 28-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,7,14-18 and 28-31* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed December 8, 2003, regarding claims 1-4, 6, 7, 14-18, and 28-31 have been fully considered but they are not persuasive. The examiner notes the thickness limitations added to claims 1, 14, 15, 17, and included in new claims 28-31. However the Yamazaki, Ma, and Goldman references also disclose dimensions for the dielectric layers which the examiner believes anticipate the applicant's invention.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 4, and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki (USPN 5,094,966).

4. With regard to claims 1, 4, and 15-18, Yamazaki (USPN 5,094,966) discloses a similar device. Figure 1 of Yamazaki illustrates a multi-terminal device in the form of a field effect transistor which has a substrate (1), a source (6), a drain (7) and a channel

region (not labeled). There is an insulating layer (5a, 5b) disposed over the channel region. There is a gate electrode (4) which is disposed over the insulating layer (5a, 5b). Yamazaki discloses (column 4, lines 46-50) that the insulating layer (5a, 5b) is made of one layer of silicon dioxide (5a) and a layer of aluminum nitride (5b). Claim 1 of Yamazaki makes it clear that the nitride layer has a thickness of 30 to 400 Angstroms (0.3 to 40 nm). The examiner believes that the Yamazaki reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

5. Claims 1, 2, 6, 14-18, and 28-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Ma et al. (USPN 6,407,435 B1).

6. In reference to claims 1, 2, and 28, Ma et al. (USPN 6,407,435 B1, hereinafter referred to as the "Ma" reference) discloses a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35). Furthermore Ma discloses that each insulating layer can be less than 5 nm thick (column 2, lines 3-4), less than 1 nm (column 6, lines 36-39), or between 0.2 and 0.5 nm (column 6, lines 36-39). The examiner believes that the Ma reference

anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

7. In reference to claim 6, Ma that the first insulating layer (170) can be silicon nitride (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35).

8. In reference to claims 14 and 29, figure 4 of Ma describes a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35). Furthermore Ma discloses that each insulating layer can be less than 5 nm thick (column 2, lines 3-4), less than 1 nm (column 6, lines 36-39), or between 0.2 and 0.5 nm (column 6, lines 36-39). The examiner believes that the Ma reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

9. In reference to claims 15, 16, and 30, Ma discloses a similar device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that

the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35). Furthermore Ma discloses that each insulating layer can be less than 5 nm thick (column 2, lines 3-4), less than 1 nm (column 6, lines 36-39), or between 0.2 and 0.5 nm (column 6, lines 36-39). The examiner believes that the Ma reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

10. In reference to claims 17, 18, and 31, Ma discloses such a multi-terminal device. Figure 4 shows a field effect transistor having a substrate (112), a source (not labeled), a drain (not labeled) and a channel region (114). There is a first insulating layer (170) and a second insulating layer (130) disposed over the channel region (114). There is a gate electrode (118) which is disposed over the second insulating layer (130). Ma states that the first insulating layer (170) can be aluminum oxide (column 4, lines 66-67 and column 5, lines 1-4). Ma states that the second insulating layer (130) can be aluminum nitride (column 4, lines 32-35). Furthermore Ma discloses that each insulating layer can be less than 5 nm thick (column 2, lines 3-4), less than 1 nm (column 6, lines 36-39), or between 0.2 and 0.5 nm (column 6, lines 36-39). The examiner believes that the Ma reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

11. Claims 1-4, 7, 14-18, and 28-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Goldman et al. (USPN 4,151,537).

12. With regard to claims 1, 4, 15-18, and 28-31, Goldman et al. (USPN 4,151,537, hereinafter referred to as the "Goldman" reference) discloses a similar device. Goldman illustrates a multi-terminal device in the form of a field effect transistor which has a substrate (12), a source (14), a drain (16) and a channel region (18). There is an insulating layer (22, 24, 26) disposed over the channel region (18). There is a gate electrode (28) which is disposed over the insulating layer (22, 24, 26). Goldman states (column 2, lines 61-65) that the top insulating layer (22) can be silicon nitride, the middle insulating layer (24) can be silicon oxynitride, and the bottom insulating layer (26) can be silicon dioxide. However, Goldman also discloses (column 2, lines 65-68) that any of the layers of the insulating layer (22, 24, 26) can be made of aluminum nitride or aluminum oxide; thereby meeting claims 1, 4, and 15-18. Goldman also discloses (column 3, lines 1-8) that the insulating layer (24) has a thickness of "up to several hundred Angstroms." The examiner believes that the Goldman reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

13. In reference to claim 2, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where the aluminum nitride is "disposed over said aluminum oxide."

14. In reference to claim 3, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where the aluminum nitride is "disposed under said aluminum oxide."

15. With regard to claim 4, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where a layer of silicon dioxide is "disposed upon said channel region, said aluminum nitride disposed over said silicon dioxide."

16. In reference to claim 7, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where a layer of silicon nitride is "disposed over said channel region, said aluminum nitride disposed under said silicon nitride."

17. In reference to claim 14, Goldman discloses a similar device. Goldman illustrates a field effect transistor which has a substrate (12), a source (14), a drain (16) and a channel region (18). There is an insulating layer (22, 24, 26) disposed over the channel region (18). There is a gate electrode (28) which is disposed over the insulating layer (22, 24, 26). Goldman states (column 2, lines 61-65) that the top insulating layer (22) can be silicon nitride, the middle insulating layer (24) can be silicon oxynitride, and the bottom insulating layer (26) can be silicon dioxide. However, Goldman also discloses (column 2, lines 65-68) that any of the layers of the insulating layer (22, 24, 26) can be made of aluminum nitride or aluminum oxide. Therefore, the examiner believes that the device of Goldman (in column 2, lines 61-68) meets the applicant's limitation where there is a "first layer comprising aluminum oxide disposed upon said channel region and a second layer comprising aluminum nitride is disposed upon said first layer." Goldman also discloses (column 3, lines 1-8) that the insulating layer (24) has a thickness of "up to several hundred Angstroms." The examiner

believes that the Goldman reference anticipates the thickness of the applicant's invention with sufficient specificity (see MPEP 2131.03 - Anticipation of Ranges).

Allowable Subject Matter

18. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggest the semiconductor device with a composite gate dielectric which includes an aluminum nitride layer with the specific additional layer structure as specified by the applicant.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ

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